IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	:	
Kee-won KWON et al.	:	Attn: Applications Branch
Serial No. [NEW]	:	Attorney Docket No. SEC.1032
Filed: 8 July 2003	:	

For: SEMICONDUCTOR MEMORY DEVICE WITH STRUCTURE PROVIDING INCREASED OPERATING SPEED

PRELIMINARY AMENDMENT

Honorable Assistant Commissioner
of Patents and Trademarks,
Washington, D.C. 20231

Sir:

Preliminary to the examination of the above-identified application, please enter the following amendments and remarks.

IN THE SPECIFICATION

Kindly amend the specification as follows:

Page 12, please replace the following paragraph with the same paragraph number:

--[00057] Hereinafter, a comparison of the structures of the semiconductor memory devices of FIGS. 5 and 6 will be described. The semiconductor memory device of FIG. 5 includes the memory array blocks 31 through 38 that are each divided into three memory sub-blocks 31a through 38a, respectively. Each memory sub-block has a memory cell of 352 bits per word line. That is, a total of twenty-four memory sub-